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EXAMINER	
RUTTEN, JAMES D	
ART UNIT	**PAPER NUMBER**
2192	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/713,652	CANTRILL, BRYAN M.	
	Examiner	Art Unit	
	J. Derek Rutten	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 have been examined.

Claim Objections

2. Claims 1 and 4 are objected to because of the following informalities:

Line 4 of claim 1 contains the words "the interrupt is enabling." This appears to be a typo where "enabling" should be changed to --enabled--.

Claim 4 recites: "The method of claim, 3." The comma appearing after the word "claim" should be placed after the number "3" as follows: --The method of claim 3,--

Appropriate correction is required.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 13-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 13 is directed to a "system for tracing." However, the claimed elements do not appear to be expressly directed to any hardware elements, and are interpreted in light of the specification (e.g. paragraph [0002]) as being software, or data structures, per se. Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component.

Data structures not claimed as embodied in computer-readable media are descriptive material per se and are not statutory because they are not capable of causing functional change in the computer. See, e.g., Warmerdam, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure per se held nonstatutory). Such claimed data structures do not define any structural and functional interrelationships between the data structure and other claimed aspects of the invention which permit the data structure's functionality to be realized. In contrast, a claimed computer-readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized, and is thus statutory. Alternatively, the "network system" of claim 21 includes hardware elements such as a processor which provides the necessary realization of functionality. Claims 14-20 are dependent upon claim 13, and are rejected for the same reasons. See MPEP 2106.01.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-12 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 1 recites the limitation "the execution control block" in lines 3-4 and 4-5. Dependent claims 2, 4, and 6-9 also contain the limitation. There is insufficient antecedent basis for this limitation in the claims. It is noted that this term is similar to "an executing control

block" which appears in line 2 of the claim. However, the term appears to correlate with the prevailing term "execution control block" which is described in paragraph [0037] of the specification. For the purpose of further interpretation, each of these terms, in particular the recitation of "executing control block" in line 2 of the claim, will be interpreted as referring to the same "execution control block" as described in the specification.

8. Claim 11 recites the limitation "wherein periodically switching...comprises" in line 3. There is insufficient antecedent basis for this limitation in the claim. For the purpose of further examination, this claim will be interpreted without the term "periodically."

9. Claim 11 recites the limitation "the first buffer and the second buffer associated with the consumer" in line 3. There is insufficient antecedent basis for this limitation in the claim. For the purpose of further examination, this claim will be interpreted as depending from claim 10 in order to provide antecedent basis.

10. Claims 2-12 are rejected as being dependent upon a rejected base claim.

11. Claim 19 recites the limitation "the consumer state" in line 2. There is insufficient antecedent basis for this limitation in the claim. For the purpose of further examination, this limitation will be interpreted without this limitation.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-7, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 2002/0199172 A1 by Bunnell (hereinafter "Bunnell") in view of US Patent Application Publication No. 2003/0084375 A1 by Moore et al. (hereinafter "Moore").

In regard to claim 1, Bunnell discloses:

A method for tracing on a processor (e.g. see Fig. 8) *comprising:*

executing an [execution] control block on the processor to obtain data,... See paragraph [0038], e.g. "trace driver."

storing the data in a first buffer, wherein the first buffer is set to active; and setting the first buffer to inactive and setting a second buffer to active, ... See paragraph [0049] e.g. "switch of the active buffer."

wherein an interrupt on the processor is disabled prior to executing the execution control block and the interrupt is [enabled] after execution of the execution control block is completed; See paragraph [0010], e.g. "interrupts must remain disabled for the duration of the trace point handling," and paragraph [0042], e.g. "interrupts are disabled." Bunnell does not expressly disclose: *...wherein the interrupt on the processor is disabled prior to switching the first buffer to inactive and the interrupt is enabling after setting the second buffer to active.* However, Moore teaches that normal programming precautions include interrupt disablement to ensure consistent results when updating components. See paragraph [0067], e.g. "interrupt disablement." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Moore's interrupt

processing with Bunnell's buffer switching in order to ensure consistent results (see Moore paragraph [0067]).

In regard to claim 2, the above rejection of claim 1 is incorporated. Bunnell further discloses: *triggering a probe in an instrumented program; and determining the execution control block associated with the probe.* See Fig. 7 and paragraph [0046], e.g. "start trigger event."

In regard to claim 3, the above rejection of claim 2 is incorporated. Bunnell further discloses: *associating the probe with a probe identifier.* See paragraph [0034], e.g. "event identification."

In regard to claim 4, the above rejection of claim 3 is incorporated. Bunnell does not expressly disclose: *wherein the determining the execution control block associated with the probe comprises querying a global array.* However, Moore teaches that a descriptor table can be used to find a handler for an interrupt. See paragraph [0007], e.g. "IDT." In Moore, a watchpoint interrupt is generated to monitor program execution by invoking an interrupt handler. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Moore's interrupt table with Bunnell's trigger event in order to find a handler (i.e. "execution control block") associated with an interrupt (i.e. triggered probe). See Moore paragraph [0007].

In regard to claim 5, the above rejection of claim 4 is incorporated. Bunnell does not expressly disclose: *wherein the probe identifier is used to query the global array.* However, Moore teaches using a interrupt identifier to query an interrupt array. See paragraph [0008], e.g. "specific IDT entry." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Moore's teaching of accessing an interrupt array with Bunnell's trigger event in order to find a service routine (i.e. "execution control block") associated with an interrupt (i.e. triggered probe). See Moore paragraph [0008].

In regard to claim 6, the above rejection of claim 3 is incorporated. Bunnell does not expressly disclose: *associating the execution control block to the probe identifier.* However, Moore teaches using a unique identifier associated with an interrupt array. See paragraph [0008], e.g. "specific IDT entry." Also see Fig. 1. elements 111 and 121. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Moore's teaching of accessing an interrupt array with Bunnell's trigger event in order to find a service routine (i.e. "execution control block") associated with an interrupt (i.e. triggered probe). See Moore paragraph [0008].

In regard to claim 7, the above rejection of claim 1 is incorporated. Bunnell further discloses: *wherein the execution control block comprises: a predicate defining criterion for executing the execution control block;* See paragraph [0038], e.g. "trace control routines;" *a consumer state component defining information associated with a*

consumer; See paragraph [0038], e.g. "trace buffers;" *and an action defining the data to be obtained from the instrumented program at the probe.* See paragraph [0038], e.g. "filter specifications."

In regard to claim 10, the above rejection of claim 7 is incorporated. Bunnell further discloses: *wherein the first buffer and the second buffer are associated with the consumer*. See paragraph [0038], e.g. "trace buffers."

In regard to claim 11, the above rejection of claim [10] is incorporated. Bunnell further discloses: *wherein [] switching the first buffer to inactive and setting the second buffer to active comprises: searching for the first buffer and the second buffer associated with the consumer using the consumer state component.* See paragraph [0039]. Trace data buffers (i.e. the consumer state component) are used to hold data before searching for and transferring to the proper buffers. No switch occurs without first using the consumer state component.

14. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell and Moore as applied to claim 5 above, and further in view of US Patent 6,848,046 to Zimmer (hereinafter "Zimmer").

In regard to claim 8, the above rejection of claim 5 is incorporated. Moore teaches that handler code (i.e. "execution control block") can be stored in a table. See

paragraph [0007]. Bunnell and Moore do not expressly disclose: *wherein the execution control block is an element in a linked list.* However, Zimmer teaches that handler code can be stored as a linked list. See column 5 lines 38-42, e.g. "linked list." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Zimmer's linked list with Moore's handler code in order to traverse a list of handlers as needed (see Zimmer column 5 lines 38-42).

In regard to claim 9, the above rejection of claim 6 is incorporated. Moore teaches that handler code (i.e. "execution control block") can be stored in a table. See paragraph [0007]. Bunnell and Moore do not expressly disclose: *wherein the execution control block further comprises: a pointer to a next execution control block.* However, Zimmer teaches that handler code can be stored as a linked list. See column 5 lines 38-42, e.g. "linked list." Each element of a linked list contains a pointer to the next element. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Zimmer's linked list pointers with Moore's handler code in order to traverse a list of handlers as needed (see Zimmer column 5 lines 38-42).

15. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell and Moore as applied to claim 1 above, and further in view of US Patent Application Publication No. 2004/0193945 by Eguchi et al. (hereinafter "Eguchi").

In regard to claim 12, the above rejection of claim 1 is incorporated. Bunnell and Moore do not expressly disclose: *wherein setting the first buffer to inactive and setting the second buffer to active occurs at a preset interval.* However, Eguchi teaches that buffers can be flushed at preset intervals. See paragraph [0075], e.g. "fixed period of time." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Eguchi's preset interval with Bunnell's buffer switching in order to commit information to memory in a concordant state after a sequence of processing (see Eguchi paragraph [0075]).

16. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell in view of "SoftFLASH: Analyzing the Performance of Clustered Distributed Virtual Shared Memory" by Erlichson et al. (hereinafter "Erlichson").

In regard to claim 13, Bunnell discloses:

A system for tracing on a processor (e.g., see Fig. 1), *comprising:*

a first buffer, wherein the first buffer is set to active; a second buffer, wherein the second buffer is set to inactive; See paragraph [0049] e.g. "switch of the active buffer."

an execution control block associated with a probe configured to obtain data from the probe; See paragraph [0045], e.g. "trace data collection control routines."

and a tracing framework configured to store the data in the first buffer and configured to set the first buffer to inactive and the second buffer to active, As above, see paragraph [0049] e.g. "switch of the active buffer."

Bunnell does not expressly disclose: *wherein the tracing framework is configured to issue a cross-call prior to setting the first buffer to inactive and the second buffer to active.* However, Erlichson teaches that cross-calls are used in synchronization processes. See page 213, column 2, 3rd paragraph, e.g. "perform a cross call to interrupt all the processors." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Erlichson's teaching of a cross call with Bunnell's buffer's in order to perform a valid synchronization as suggested by Erlichson.

In regard to claim 14, the above rejection of claim 13 is incorporated. Bunnell further discloses: *an instrumented program comprising the probe.* See Abstract, e.g. "dynamically instrumented."

In regard to claim 15, the above rejection of claim 13 is incorporated. Bunnell further discloses: *a consumer associated with the first buffer and the second buffer.* See Fig. 1, element 22 "Trace Collector."

17. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell and Erlichson as applied to claim 13 above, and further in view of Moore.

In regard to claim 16, the above rejection of claim 13 is incorporated. Bunnell and Erlichson do not expressly disclose: *wherein the cross-call comprises disabling an interrupt on the processor prior to setting the first buffer to inactive and enabling the*

interrupt after setting the second buffer to active. However, Moore teaches that normal programming precautions include interrupt disablement to ensure consistent results when updating components. See paragraph [0067], e.g. "interrupt disablement." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Moore's interrupt processing with Bunnell's trace execution and storage in order to ensure consistent results (see Moore paragraph [0067]).

18. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell and Erlichson as applied to claim 13 above, and further in view of DeWitt.

In regard to claim 17, the above rejection of claim 13 is incorporated. Bunnell and Erlichson do not expressly disclose: *wherein the tracing framework is configured to disable an interrupt prior to obtaining data from the probe and enable the interrupt after obtaining data from the probe.* However, DeWitt teaches that tracing software usually disables interrupts during operations and enables when it has completed operations. See paragraph [0011], e.g. "disables interrupts." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use DeWitt's interrupt processing with Bunnell's trace execution and storage in order to prevent interrupts from disrupting trace processing (see DeWitt paragraph [0011]).

In regard to claim 18, the above rejection of claim 13 is incorporated. All further limitations have been addressed in the above rejection of claim 7.

In regard to claim 19, the above rejection of claim 18 is incorporated. Bunnell further discloses: *wherein the tracing framework is configured to obtain the execution control block associated with the probe []*. See Fig. 7 and paragraph [0046], e.g. "start trigger event."

19. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell and Erlichson as applied to claim 13 above, and further in view of US Patent 6,952,664 to Lahiri et al. (hereinafter "Lahiri").

In regard to claim 20, the above rejection of claim 13 is incorporated. Bunnell and Erlichson do not expressly disclose: *wherein the first buffer comprises a drop count.* However, Lahiri teaches the use of a "touch count" with a buffer. See column 7 line 58 – column 8 line 3. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Lahiri's touch count with Bunnell's buffer in order to determine a threshold for that buffer as suggested by Lahiri (see column 7 line 67 – column 8 line 3).

20. Claims 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell in view of Erlichson in view of US Patent Application No. 2003/0056200 A1 by Li et al. (hereinafter "Li").

In regard to claim 21, Bunnell discloses:

A network system having a plurality of nodes (See Fig. 1), *comprising:*

a processor; See Fig. 1 element 12, "Target Computer."

a first buffer associated with the processor, See Fig. 1. element 24 "Start Buffer."

wherein the first buffer is set to active; See paragraph [0049] e.g. "switch of the active buffer."

a second buffer associated with the processor, See Fig. 1. element 26 "Main Buffer."

wherein the second buffer is set to inactive; See paragraph [0049] e.g. "switch of the active buffer." Note that a switch of the active buffer requires that the currently active buffer becomes inactive.

an execution control block associated with a probe configured to obtain data from the probe; See paragraph [0045], e.g. "trace data collection control routines."

and a tracing framework configured to store the data in the first buffer and configured to set the first buffer to inactive and the second buffer to active, See Fig. 1, as above. Also paragraph [0029], e.g. "trace environment."

Note that Bunnell discloses a "network" consisting of a host system and a target system, wherein the execution of target code occurs on the target computer. Bunnell does not expressly disclose:

wherein the tracing framework is configured to issue a cross-call prior to setting the first buffer to inactive and the second buffer to active;

wherein the processor executes on any node of the plurality of nodes, wherein the first buffer executes on any of the plurality of nodes, wherein the second buffer executes on any of the plurality of nodes, wherein the execution control block executes on any of the plurality of nodes, and wherein the tracing framework executes on any of the plurality of nodes.

However, Erlichson teaches that cross-calls are used in synchronization processes. See page 213, column 2, 3rd paragraph, e.g. "perform a cross call to interrupt all the processors." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Erlichson's teaching of a cross call with Bunnell's buffer's in order to perform a valid synchronization as suggested by Erlichson.

Further, Li teaches execution and tracing of target code on a plurality of nodes. See paragraph [0059], e.g. "traced across processes and over multiple processing devices." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Li's teaching of tracing on a plurality of nodes with Bunnell's processor, buffers, execution control blocks, and tracing framework, in order to provide cross-process causal tracing as suggested by Li (see paragraph [0059]).

In regard to claim 23, the above rejection of claim 21 is incorporated. All further limitations have been addressed in the above rejection of claim 7.

21. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell, Erlichson and Li as applied to claim 21 above, and further in view of Moore.

In regard to claim 22, the above rejection of claim 21 is incorporated. Bunnell further discloses disabling interrupts. See paragraph [0042], e.g. "interrupts are disabled." Bunnell, Erlichson, and Li do not expressly disclose: *wherein the cross-call comprises disabling an interrupt on the processor prior to setting the first buffer to inactive and enabling the interrupt after setting the second buffer to active.* However, Moore teaches that normal programming precautions include interrupt disablement to ensure consistent results when updating components. See paragraph [0067], e.g. "interrupt disablement." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Moore's interrupt processing with Bunnell's buffer switching in order to ensure consistent results (see Moore paragraph [0067]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Derek Rutten whose telephone number is (571)272-3703. The examiner can normally be reached on M-F 7:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571)272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

jdr

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